Heterogeneous Embedded Systems Very Large Scale Design Space Exploration

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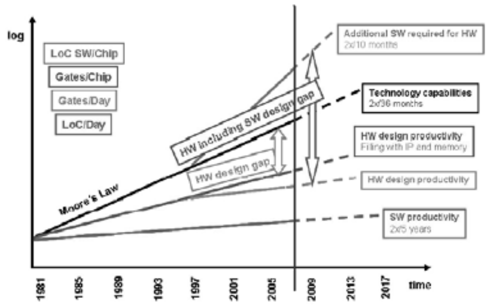
Outline

1. ITRS Roadmap and challenges ahead
2. Design Space Exploration: Architecture, Physical Design, Compiler, Applications
3. Simulation Based *vs* Emulation Based DSE: The Trend
4. DES on Large Scale Emulation Platform
5. EVE Emulation Platform
6. Small Scale Single FPGA Chip Multiprocessor
7. DSE and GALS: Interchip and Meso link
8. Conclusion

ITRS Roadmap 2007



Hardware and Software Design Gaps Versus Time

Source ITRS 2007

• Design productivity with growing silicon complexity and system complexity: *« most massive and critical DT challenge both near and long term »*

• Implied needs: (1) verification (2) reliable and predictable silicon implementation (3) embedded software design

Heterogeneous Multiprocessor Design Space Exploration : Architecture

Feature	P #1	P #2	…..	P #N
I Cache (size, org.)				
D Cache (size, org.)				
Local Mem				
FU integer				
FU FP				
HW Accelerators (connection mode)				
…..				
Internal core Width, pipeline				

NOC Feature	NOC #1	NOC #m
Switch architecture Arbitration Buffers		
Topology Regular heterogeneous		
Clock domains islands		
Flow control		
…..		
routing		

Heterogeneous Multiprocessor Design Space Exploration : Compiler

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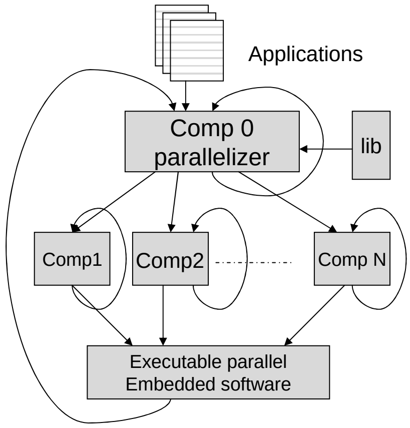
Feature	P #1 Comp #1	P #2 Comp #2	…..	P #N Comp #N
D cache optimization				
I Cache optimization				
Local Mem optimization				
Instruction Scheduling/regAllocation				
Fine grain concurrency				
…..				
Loop parallelism				



Automatic Design Space Exploration of Automatic Parallelization techniques with compilers hierarchy

Heterogeneous Multiprocessor Design Space Exploration : Place and Route

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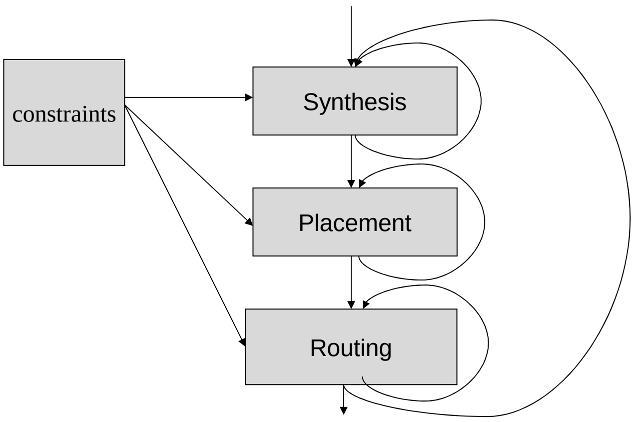
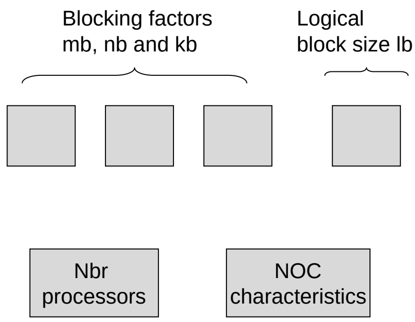


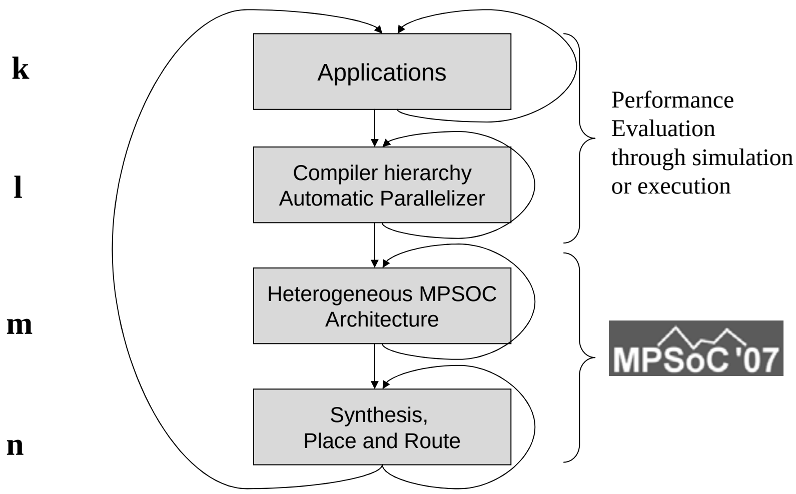
Heterogeneous Multiprocessor Design Space Exploration : Applications

- Design space exploration apply to applications
- Application tuning well known in for example ScaLAPACK, PETSc
- Example PDGEMM
- *mb*, *nb* and *kb* blocking factors of the block-cyclic distribution of matrices A, B and C
- Blocking factor bf implies that blocks of size *bf* x *bf* of matrix M are distributed cyclicly
- Logical block size *lb* implies for a given processor to gather *lb* rows of A and *lb* columns of B and generate *lb x lb*



Best value for logical block size is machine dependent

Very Large Scale DSE



VLS-DSE

$$\text{VLS-DSE}_{sim} = k \times l \times \text{SimEval}_{cycles} = k \times l \times S_{up}\text{Emulcycles}$$

$$\text{VLS-DSE}_{emul} = k \times l \times \text{EmulEval}_{cycles} + N \times [(\text{genarch} + \text{spr})]$$

$N = \text{Max}(m, n)$

$$k \times l \times S_{up}\text{EmulEval}_{cycles} > k \times l \times \text{EmulEval}_{cycles} + N \times [(\text{genarch} + \text{spr})]$$

$$(S_{up} - 1) \times k \times l \times \text{EmulEvalcycles} > N \times [(\text{genarch} + \text{spr})]$$

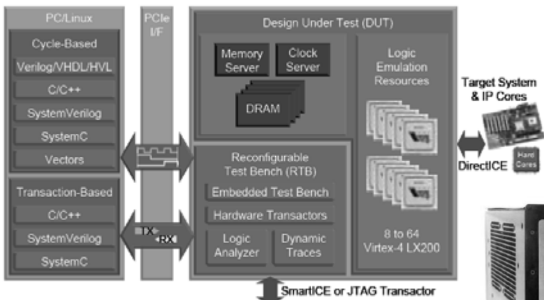
$$(S_{up} - 1) \times k \times l \times \text{EmulEvalcycles} > N \times [G \times \text{EmulEvalcycles}]$$

$$\mathbf{(Sup - 1) \times k \times l > N \times G}$$

More embedded software: more k and l
Moore's law: Sup will increase
2008 : Sup ~ 10,000

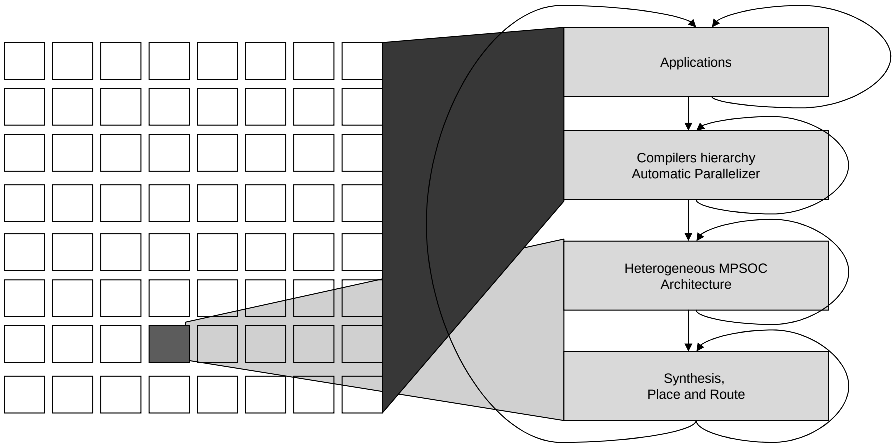
G ? Reduce inter-tiles variations and reuse small scale multiprocessor IP

EVE Emulator Environment Specifications



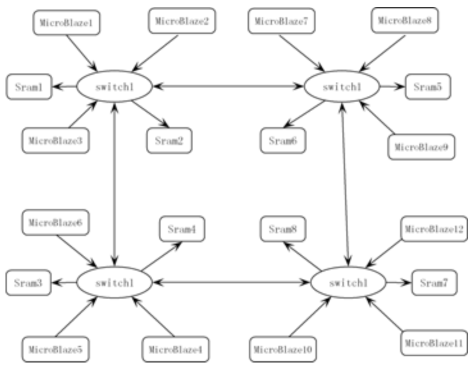
Features	Descriptions
Logic capacity per box	• 12.5M to 100M ASIC gates
Max interconnected boxes	• Up to 2 boxes with max design capacity of 200M ASIC gates
On-board large memory	• 4 independent banks of 1GBytes each with 2 ports per bank
On-module fast memory	• 4 independent banks of 64MBytes each with 2 ports per bank
DirectICE interface	• 1,000 unmultiplexed I/O pins + 8 clock inputs • Up to two DirectICE interfaces
SmartICE interface	• 64 I/O pins + 4 clocks
System interfaces supported via transactors	• DRAM, FLASH, LCD, DTV, UART, JTAG, PCIe, Ethernet, USB, etc.

Heterogeneous MPSOC on Large Scale Emulation Platform



DSE Execution Time/Support Driven MPSOC Architecture Design

Single FPGA Chip Small Scale Multiprocessor

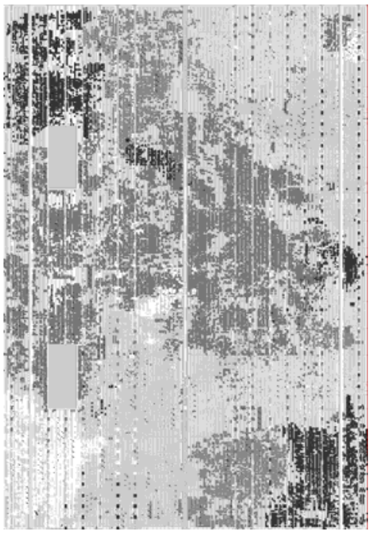


IP component	description	source	version	Qty
Processor	Soft core IP	Microblaze Soft core IP Xilinx	5.00 b	12
Memory	Soft core IP	Xilinx Coregen 96KB	v.2.4.	8
Network on chip switch	Soft core IP	VHDL Arteris Danube library	1.10	4
Interchip	Soft core IP	VHDL Arteris Danube library	1.10	1

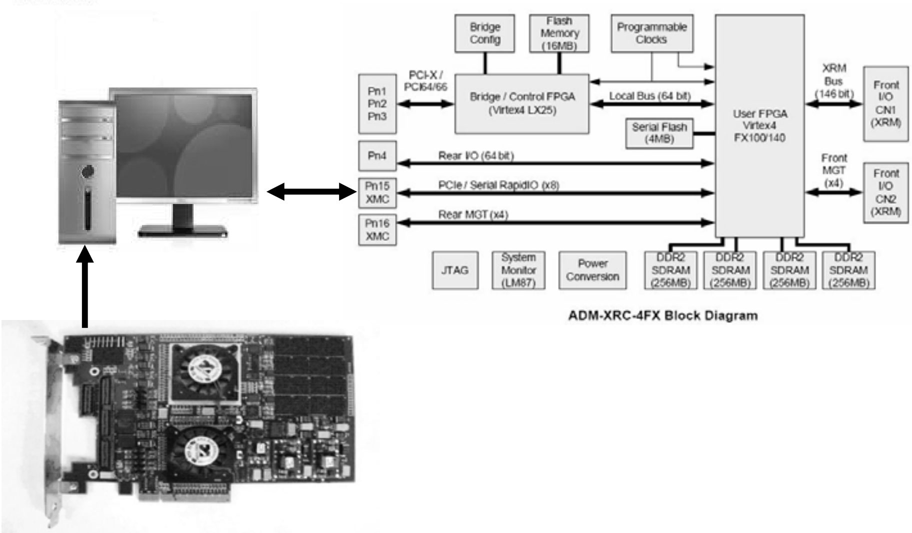
Implementation of Small Scale Multiprocessor

FPGA Resource Xilinx Virtex-4 FX-140	Utilization	%
Number of DSP48s	**36**/192	18
Number of RAMB16s	**53**/552	97
Number of Slices	**25261**/63168	56
Number of SLICEMs	**2795**/31584	8

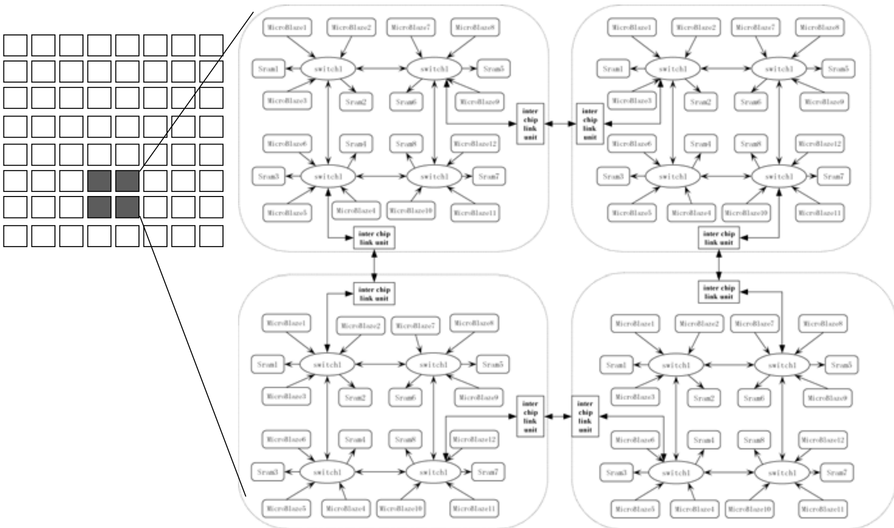
Frequency 80 Mhz



Alpha-Data Board ADM-XRC



Emulator Sensitive Simple Extension Example



GALS: Interchip and Meso link

- Chip multiprocessor may work with multiple clocks domains for various architectural components (processor, network on chip, memory controller)
- Heterogeneous multiprocessors have natural multiple clocks domains
- VLS-DSE exploit frequency islands for local DSE

Logical/Circuit/Physical Design Technology Requirements—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
Asynchronous global signaling: % of a design driven by handshake clocking	7%	11%	15%	17%	19%	20%	22%	23%	25%
Parameter uncertainty: %-effect (on signoff delay)	6%	8%	10%	11%	11%	12%	14%	15%	18%
Simultaneous analysis objectives: # of objectives during optimization	4	5	6	6	6	6	7	8	8
Circuit families: # of families in a single design	3	3	4	4	4	4	4	4	4
Synthesized analog content: % of total design analog content	15%	16%	17%	18%	19%	20%	23%	25%	28%
Full-chip leakage (normalized to full-chip leakage power dissipation in 2007)	1	1.5	2	2.5	2.75	3	3.5	4	6

Source ITRS 2007

Dealing with MPSOC Design and GALS

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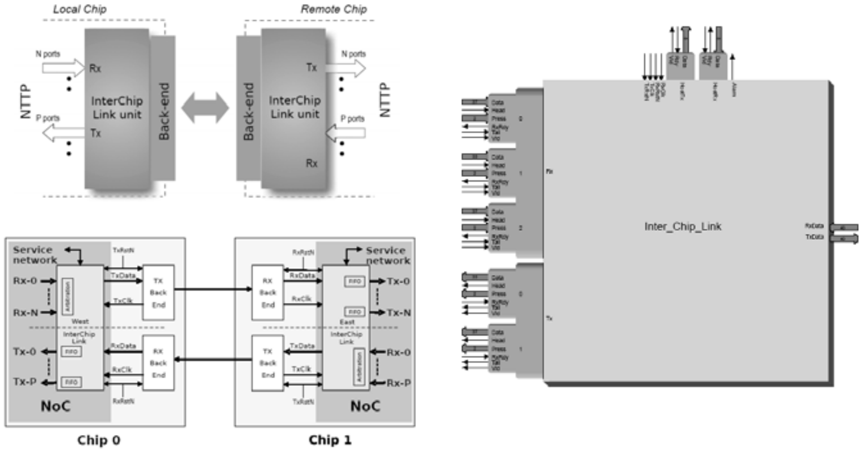

Arteris Interchip Link

Dealing with MPSOC Design and GALS

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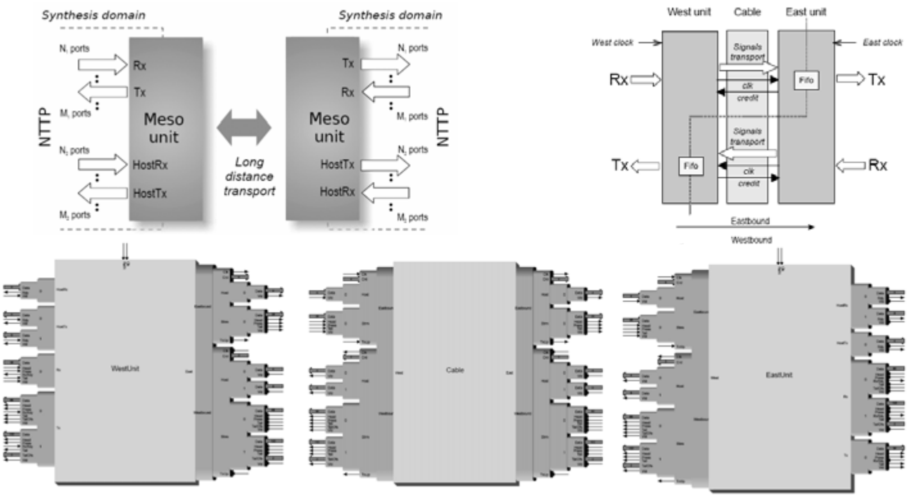
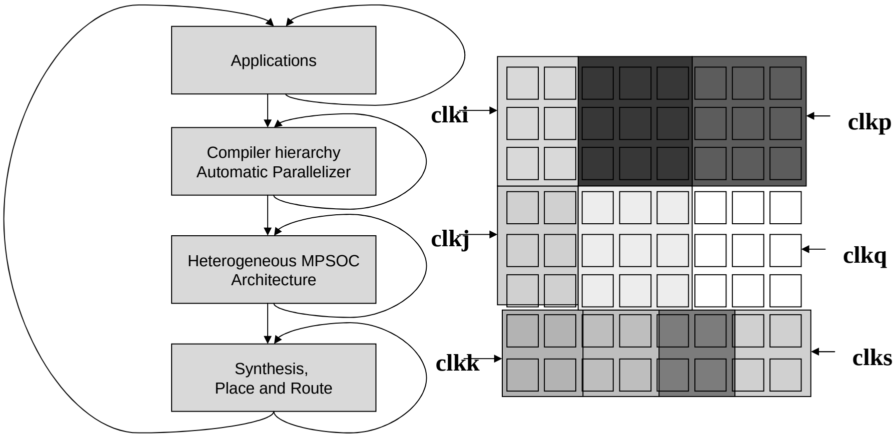


Arteris Meso Unit

GALS Multiprocessor Modelling on Large Scale Emulation Platform



Multi-chip Frequency Islands Partitionning
With performance and area constraints

Conclusion

- Heterogeneous MPSOC requires very large scale design space exploration (increasing heterogeinity increase design space)
- Large scale emulation platform is the only tool for billion cycle evaluation in reasonnable performance evaluation time
- Reasonnable performance evaluation time is design space size dependent

Single Chip Multiprocessor Design Space Size

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Architecture + Physical design + Compiler + Applications

- This work : quick ramp up of large scale multiprocessors from single chip multiprocessors with design space exploration on large scale emulation platform
- Future work: automatic design space exploration and 3D

Thank you for attention.
Questions ?

We wish to thank EVE

for their excellent support.

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